X64-CL™ Full

KEY FEATURES

- Acquires images from one Base, Medium or Full Camera Link camera
- Rapid image acquisition rates up to 680 MB/s and high-speed image transfer to host memory at 528MB/s
- Up to 2GB local frame buffer
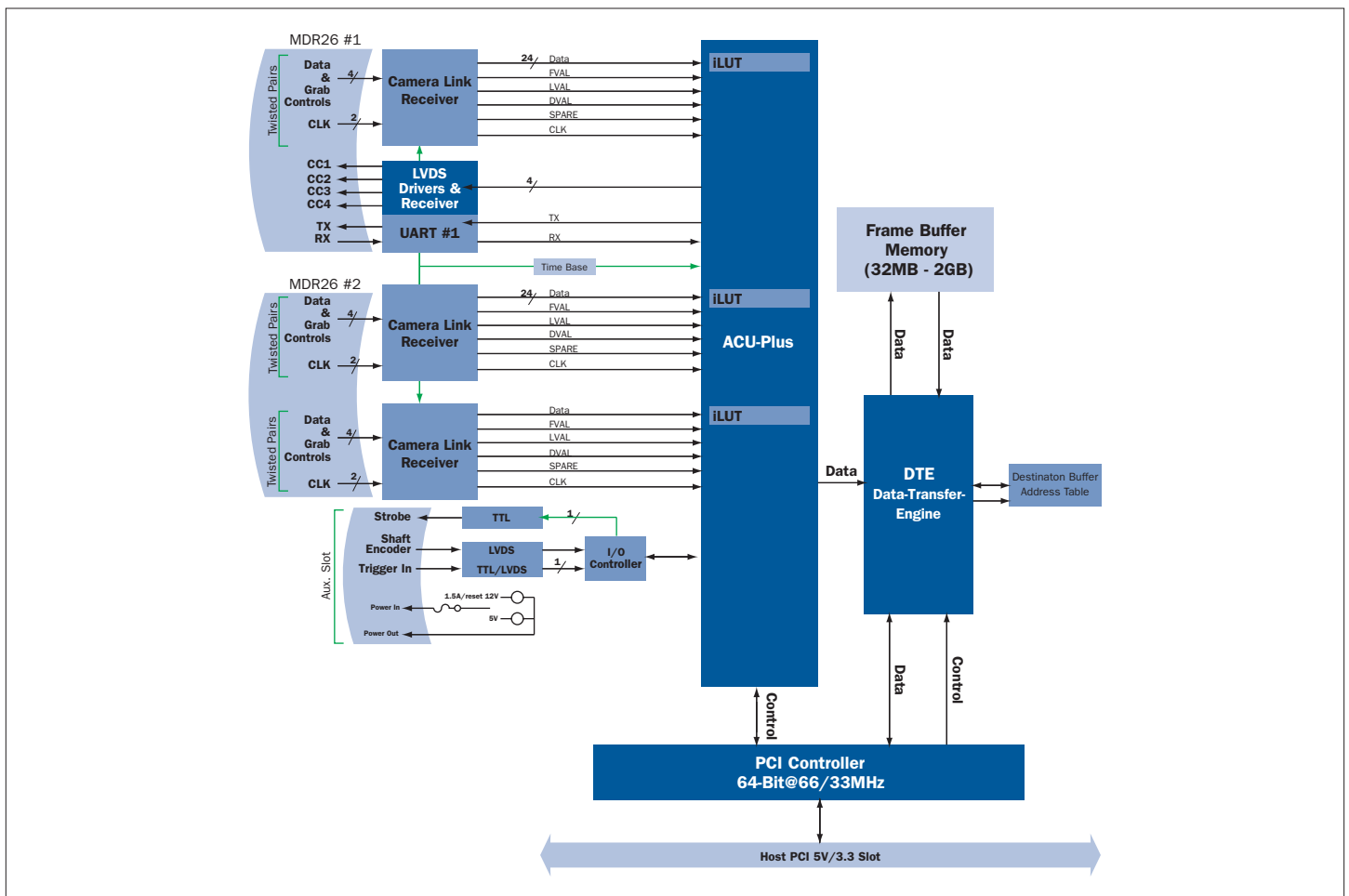- Supports Camera Link operations up to 85MHz

OVERVIEW

Camera Link™ frame grabber
for high speed machine vision

Compatible with one Base, Medium or Full Camera Link camera, the X64-CL Full is universal PCI slot compliant and supports all standard multiple tap area and linescan color and monochrome Camera Link cameras. For greater versatility, the X64-CL Full can also interface with custom camera formats, including pixel depths and tap configurations not covered by the Camera Link standard.

The X64-CL Full has been built within DALSA's Trigger-to-Image Reliability technology framework. Trigger-to-Image Reliability leverages DALSA's hardware and software innovations to control, monitor and correct the image acquisition process from the time that an external trigger event occurs to the moment the data is sent to the PCI bus. Trigger-to- Image Reliability enables more efficient and reliable machine vision inspections by securing the image acquisition process, providing traceability when errors do occur and permitting recovery from those errors.

DALSA

MDR26 #1

Twisted Pairs

Data & Grab Controls — 4
CLK — 2

Camera Link Receiver

24 / Data
FVAL
LVAL
DVAL
SPARE
CLK

iLUT

CC1
CC2
CC3
CC4

LVDS Drivers & Receiver

4 /

TX
RX

UART #1

TX
RX

Time Base

MDR26 #2

Twisted Pairs

Data & Grab Controls — 4
CLK — 2

Camera Link Receiver

24 / Data
FVAL
LVAL
DVAL
SPARE
CLK

iLUT

ACU-Plus

Twisted Pairs

Data & Grab Controls — 4
CLK — 2

Camera Link Receiver

Data
FVAL
LVAL
DVAL
SPARE
CLK

iLUT

Frame Buffer Memory (32MB - 2GB)

Data   Data

Aux. Slot

Strobe → TTL — 1 /
Shaft Encoder → LVDS
Trigger In → TTL/LVDS — 1 /

I/O Controller

Power In — 1.5A/reset 12V
5V
Power Out

Data

DTE Data-Transfer-Engine

Destinaton Buffer Address Table

Data   Control

Control

PCI Controller 64-Bit@66/33MHz

Host PCI 5V/3.3 Slot

X64-CL Full - Functional Block Diagram

Unprecedented Acquisition Control

Successful industrial machine vision applications require consistent and predictable results in demanding operating environments. The X64-CL Full Acquisition Control Engine (ACU), delivers an unprecedented level of acquisition functionality. The X64-CL Full not only provides the industry's most flexible front-end for interfacing Camera Link cameras, it also incorporates a fault tolerant image synchronization design, allowing it to automatically detect report and recover from a lost camera
signal ensuring a greater level of reliability within the imaging sequences.

The X64-CL Full gives machine vision application developers the ability to combine color and monochrome acquisition on a single board. Developers can perform critical pixel transformations during the acquisition process saving valuable preprocessing time.

Embedded timing logic within the ACU identifies each acquired image with a time code, allowing image data to be readily correlated with physical objects on the production line.

Capable of acquiring images at rates up to 255MB/s per channel (510MB total), the X64-CL Full makes image acquisition from the new generation of CMOS and multi-tap CCD camras more efficient and cost effective. The board supports fixed and variable size frames ranging up to 256KB horizontal pixels per line and up to 16 million vertical lines per frame for area scan cameras. Precise timing controls allow frame size adjustments in steps of 8 pixels/step for horizontal lines and in steps of one line/step vertically.

In conjuction with an onboard quadrature shaft-encoder input, the ACU acquires images from a linescan camera at a rate that is locked to the speed of the web. The X64-CL shaft-encoder feature now supports cascaded divide and multiply to further increase the step resolution. More accurate step resolution results in a higher quality image that makes processing algorithms more accurate and tolerant to motion artifacts. One feature of particuliar interest to OEMs developing web-scanning applications is the X64-CL's ability to support infinite length frames from a linescan camera, which enables 100 percent line capture as well as repeatable accuracy and faster execution times.

Optimized Data-Transfer

Delivering fast and secure data transfer with zero CPU usage, the X64-CL Full's Data Transfer Engine (DTE) features high speed memory interface, multiple independent Direct Memory Access (DMA), and onboard tap descriptors, the DTE's powerful architecture delivers robust performance for critical machine vision tasks.

The DMAs allow the DTE to transfer images from the acquisition control unit to local frame buffer memory, or transfer the same image to multiple addresses in the host memory. The ACU and DTE use the onboard memory to perform these operations concurrently, yet at different rates, yielding optimal utilization of system bandwidth. Moreover, the X64-CL Full now supports up to 2GB of onboard memory for higher speed frame rate cameras.

Designed to simplify machine vision tasks, the DTE is also responsible for on-the-fly input tap adjustments for directions, pixel overlap and under lap. This enables the DTE to deliver images that are ready for processing while freeing up the host CPU for other image analysis tasks.

Conventional PCI bus transfers utilizing scatter-gather techniques rely on the CPU to load the host frame buffer destination memory addresses during live acquisition, which increases the load on the CPU and slows image-processing tasks. The DTE offloads this task by using a sophisticated control unit to automatically capture and store the destination frame buffer addresses from the host memory. In addition, the control unit performs autonomous and robust image transfers to ensure data integrity during continuous image acquisition in non-real-time operating systems, such as Windows®XP, Windows®2000 and Windows NT®.

Camera Support

The X64-CL Full is compatible with one Full, one Medium or one Base Camera Link area or linescan mono or RGB camera. In addition, the X64-CL Full provides optional support for non-Camera Link formats and acquisition from two synchronized Base cameras. It further supports custom camera formats such as four 14/16-bit taps and ten 8-bits/tap1.

Visual Status LED

The X64-CL Full further facilitates ease-of-use by utilizing visual status LEDs, mounted on the card's bracket, to simplify system installation and setup. A status indicator LED provides visual feedback when the correct camera connection is made and when a grab is in progress; a second LED shows when a valid external trigger is detected. These visual indicators allow developers to instantly recognize if cabling has been correctly set up greatly facilitating the diagnostic process.

External Event Synchronization

The X64-CL Full features a trigger input, along with strobe and exposure control output signals, to synchronize image captures with external events.

RS-232 Communications Ports

The X64-CL Full features an onboard "Serial" serial port that provides integrated support for camera control and setup for machine vision applications. PC-independent in nature, this communication port can be used with off-the-shelf communication utilities such as HyperTerminal to control and configure Camera Link cameras with ease and without requiring additional external cabling.

Software Support
Acquisition, processing and analysis

The X64-CL Full is fully supported by DALSA's Sapera™ LT software development libraries enabling applications to be developed under Windows NT®, Windows®2000, and Windows®XP. Sapera LT allows users to develop applications with C language DLLs, C++® classes or Active X®controls for Microsoft®Visual C/C++®6.0 (or higher) or Visual Basic® 6.0 (or higher) development platforms.

Sapera LT's advanced image acquisition and control functions are an integral part of DALSA's stringent Trigger-to-Image Reliability technology framework. Sapera LT offers users a single API across DALSA's current and future hardware platform, to deliver a comprehensive feature set including program portability, versatile camera controls, flexible display functionality and management, and easy to use application development wizards.

Sapera LT (ver. 5.0) comes bundled with DALSA's advanced CamExpert, a proprietary camera configuration utility specifically designed to leverage the power of DALSA's image acquisition boards. This Windows-based utility provides an interactive environment within which to create a new, or modify an existing, configuration file for area and linescan applications.

For image processing and analysis DALSA offers Sapera Processing. Fully integrated with Sapera LT functionality, Sapera Processing is a dynamic Windows-based comprehensive programming library. Hardware independent and designed to simplify vision application development, Sapera Processing is based on a set of high performance C++ classes and uses MMX, SSE (streaming SIMD Extensions), and SSE2 to meet the challenging operational requirements of today's imaging systems. Scalable in design, Sapera Processing offers a comprehensive set of optimized tools, available as a suite or standalone, including image processing, search (pattern matching), OCR, barcode decoding, and blob analysis. Sapera LT and Sapera Processing combine seamlessly to deliver a powerful and easy to use development resource for advanced image acquisition, processing, and analysis.

Specifications*

Board	•Half length PCI 2.1 64-bit 66MHz compliant •5V and 3.3V slot compatible

Acquisition	•Acquisition rates up to 680MB/s
	•Horizontal Size (min/max): 8 byte/256KB
	•Vertical Size (min/max):
	       Linescan cameras: 1 line to infinity
	       Area scan cameras: 1 line to 16 million/frame
	                  variable length frames
	•Onboard frame buffer memory up to 2GB (32MB standard)
	•LUT: One 8 or 10-bit(mono/RGB) or 12-bit (mono) input lookup table[1]

Pixel Formats Transfers	•Single slot solution supports 1 Medium, 1 Base or 2 synchronized Base Camera Link cameras
	•Interfaces to digital area scan or linescan color or monochrome cameras
	•Supports standard multi-tap Camera Link configurations:
	       1 Full camera: 8 x 8-bit
	       1 Medium camera: 4 x 8-bit, 4 x 10-bit, 4 x 12-bit, 1 x 30-bit/RGB and 1 x 36-bit
	       1 Base camera: 3 x 8-bit, 2 x 10-bit, 2 x 12-bit, 1 x 14-bit, 1 x 16-bit, and 1 x 24-bit/RGB
	•Alternate multi-tap Camera Link configurations support: 4 x 14-bit, 4 x 16-bit, 1 x 48-bit or 1 x 64-bit
	•Monochrome 8, 10, 12, 14, 16, or 36-bit/RGB
	•Real-time transfers to system memory:
	       PCI-32 bus: 32 bits @ 33MHz
	       PCI-64 bus: 64 bits @ 66MHz
	       PCI-X bus: 64 bits @ 66MHz
	•On-the-fly tap adjustments for multiple tap area scan and linescan cameras

Controls	•Comprehensive event notification includes start/end-of-frame, sequence or N-line events •One independent TTL/LVDS trigger input programmable as active high or low (edge or level trigger) •One strobe TTL output for area scan and linescan cameras •One PC independent "serial communication" port provides seamless interface to MS Windows applications •Quadrature (AB) shaft-encoder inputs for external web synchronization; supports cascaded divide and multiply
Power Output	•Power-on-reset fused +12V/+5V DC output at 1.5A
Software	•Microsoft Windows NT 4.0, Windows 2000, and Windows XP compliant •Full support of the Sapera programming package •Compatible with Microsoft Visual Studio 6.0 and .Net (unmanaged code only), Visual Basic 6.0 and Borland C++ Builder 5.5 or higher
System Requirements	•PCI-64 or PCI-32 compliant system and 64MB system memory
Dimensions	•8.27" (21cm) Length x 4.20" (10.7cm) Height
Temperature	•0° C (32° F) to 55° C (131° F) •Relative Humidity: up to 95% (non-condensing)
Markings	•FCC class B - approved •CE class B - approved

* Last updated September 2006   Specifications subject to change without notice

Notes:

1. 8-bit: 8 taps max in monochrome or 2 taps max in RGB mode; 8-in/8-out

    10-bit: 4 taps max in monochrome or 1 tap max in RGB mode; 10-bit in/10 or 8-bit out;

    12-bit: 2 tap max; 12-bit in/12 or 8-bit out; available on models with 32MB and 128MB frame buffer memory

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